

Program Verification

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Joint work with:

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- ➡ Filip Konecny (PhD 2008-2012, now at EPFL, Lausanne)
- ➡ Jiri Simacek (PhD 2008-2012, now at NetSuite, Brno)
- ➡ Florent Garnier (PostDoc 2010-2012, now at MathWorks, Paris)

Program Verification Timeline



Program Verification Timeline

Hilbert's
Program

≤ 1920



Program Verification Timeline

Hilbert's
Program

Computability

≤ 1920 1931-1936



Program Verification Timeline

Hilbert's
Program

Computability

Hoare Logic

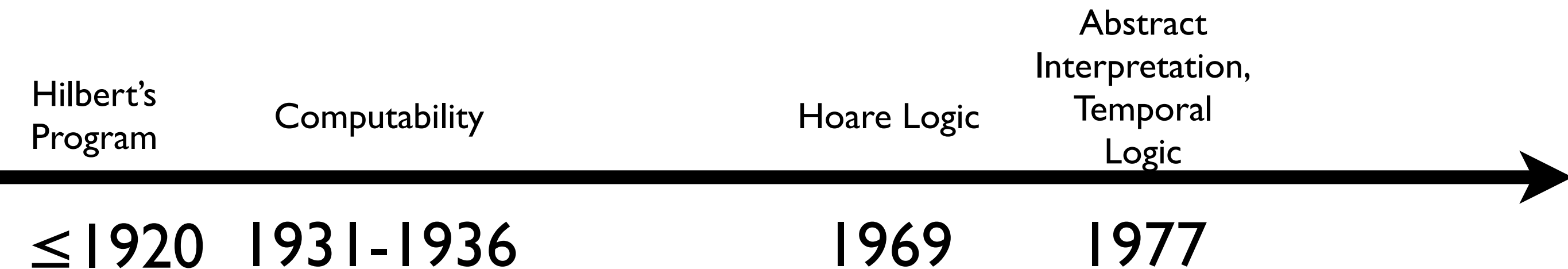
≤ 1920

1931-1936

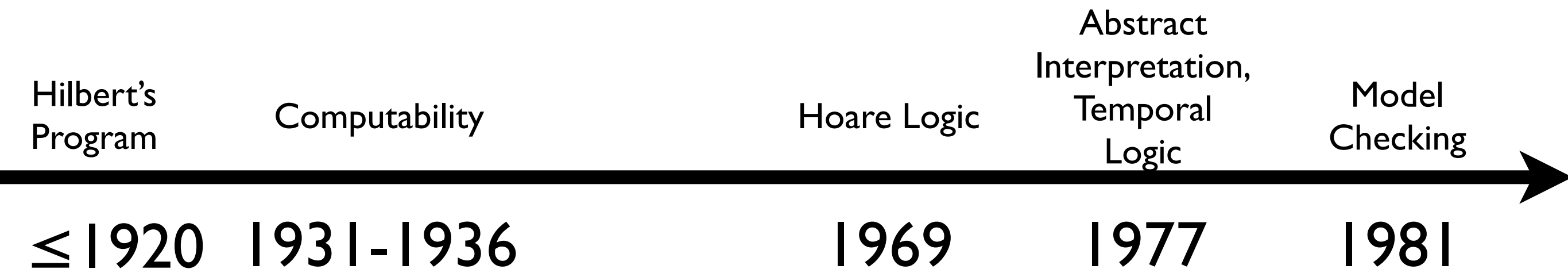
1969



Program Verification Timeline



Program Verification Timeline



Program Verification Timeline



Program Verification Timeline



Program Verification Timeline

SLAM
if=nodes->(); i ++ visproc, end() * node; {

2000



Program Verification Timeline

SLAM
if=nodes->(); i ++ visproc, end() * node; {

Astrée

2000

2001-2010



Program Verification Timeline

SLAM
if=node->(); i ++ vis; end(); node;{
procs,

Astrée

SLAYER

2000

2001-2010

2006-2013

Program Verification Timeline

SLAM
if=node->(); i++; visit_procs; end(); node;}

Astrée

SLAYER

2000

2001-2010

2006-2013

Reports of 100K to 10 million lines of verified code!

Program Verification Timeline

SLAM
if=node->(); i++; visit_procs; end(); node;}

Astrée

SLAYER

SV-COMP

2000

2001-2010

2006-2013

2012≤

Reports of 100K to 10 million lines of verified code!

Program Verification Status

Static Analysis






Model Checking



- Lots of false positives
- No automatic refinement
- Infinite state spaces
- No guarantee of termination

What's wrong ?

-  The success criteria are wrong
-  The size of a program gives no indication on the complexity of its verification problems
-  Empirical success stories (deadly bug found in device driver) are almost impossible to reproduce and trust

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We need better measures of problem complexity than the
of lines, or the # of variables, etc ...


A Personal Timeline



A Personal Timeline

Logics for
Shape Analysis

02-04

A thick black horizontal line with a triangular arrowhead pointing to the right, spanning the width of the slide.

A Personal Timeline

Logics for
Shape Analysis

02-04

Quantitative
Shape Analysis

05-07



A Personal Timeline

Logics for
Shape Analysis

02-04

Quantitative
Shape Analysis

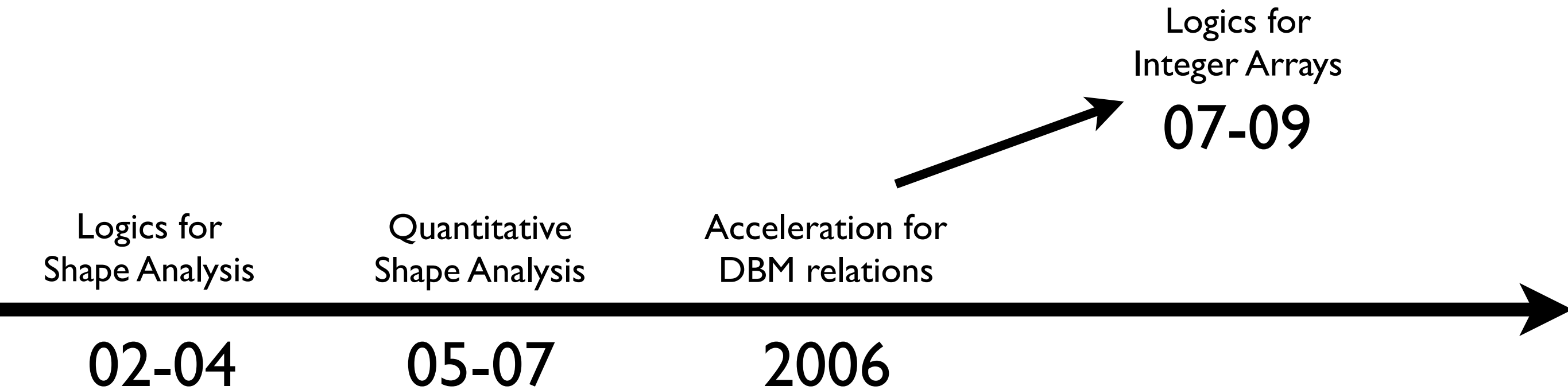
05-07

Acceleration for
DBM relations

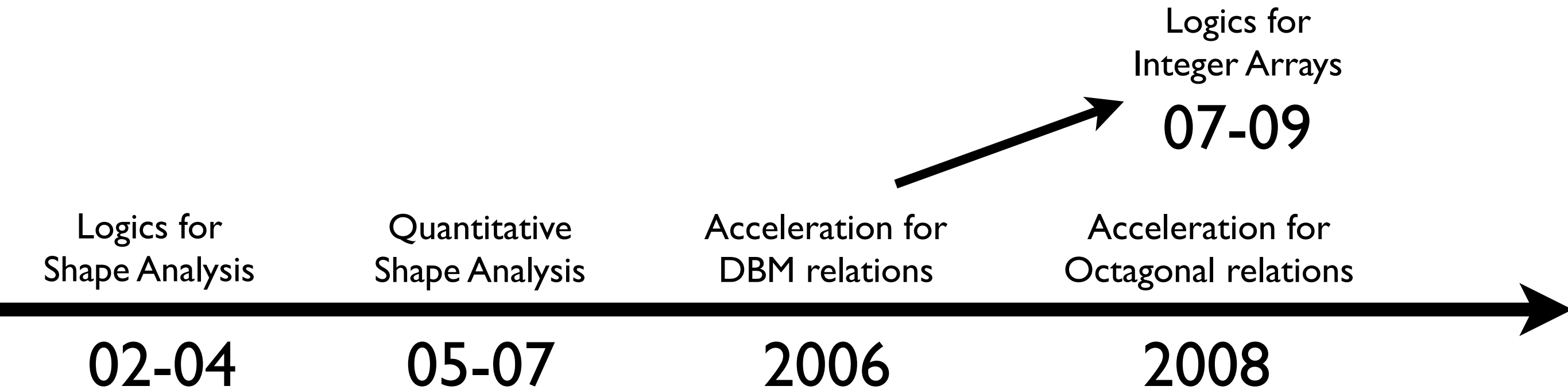
2006



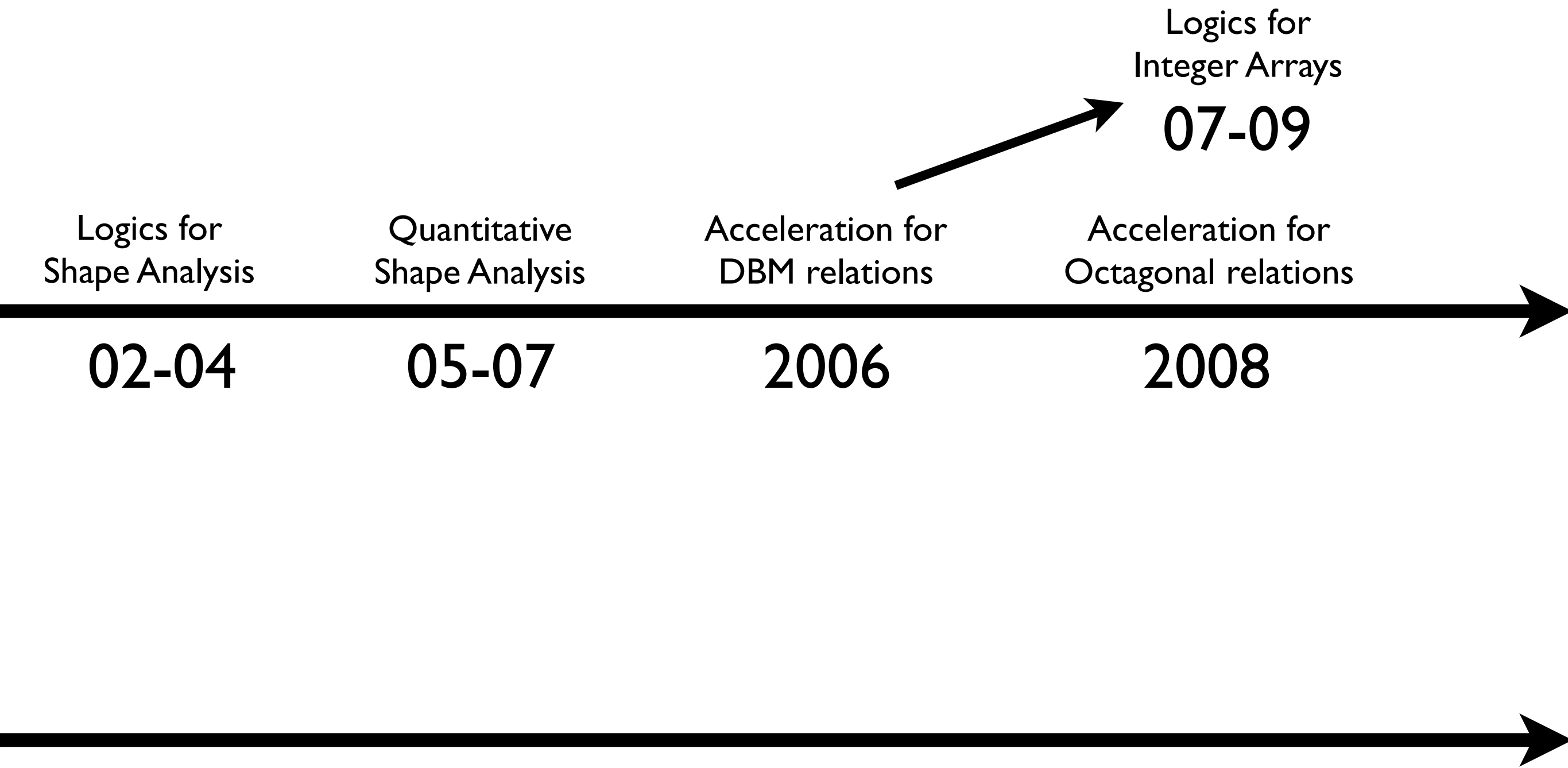
A Personal Timeline



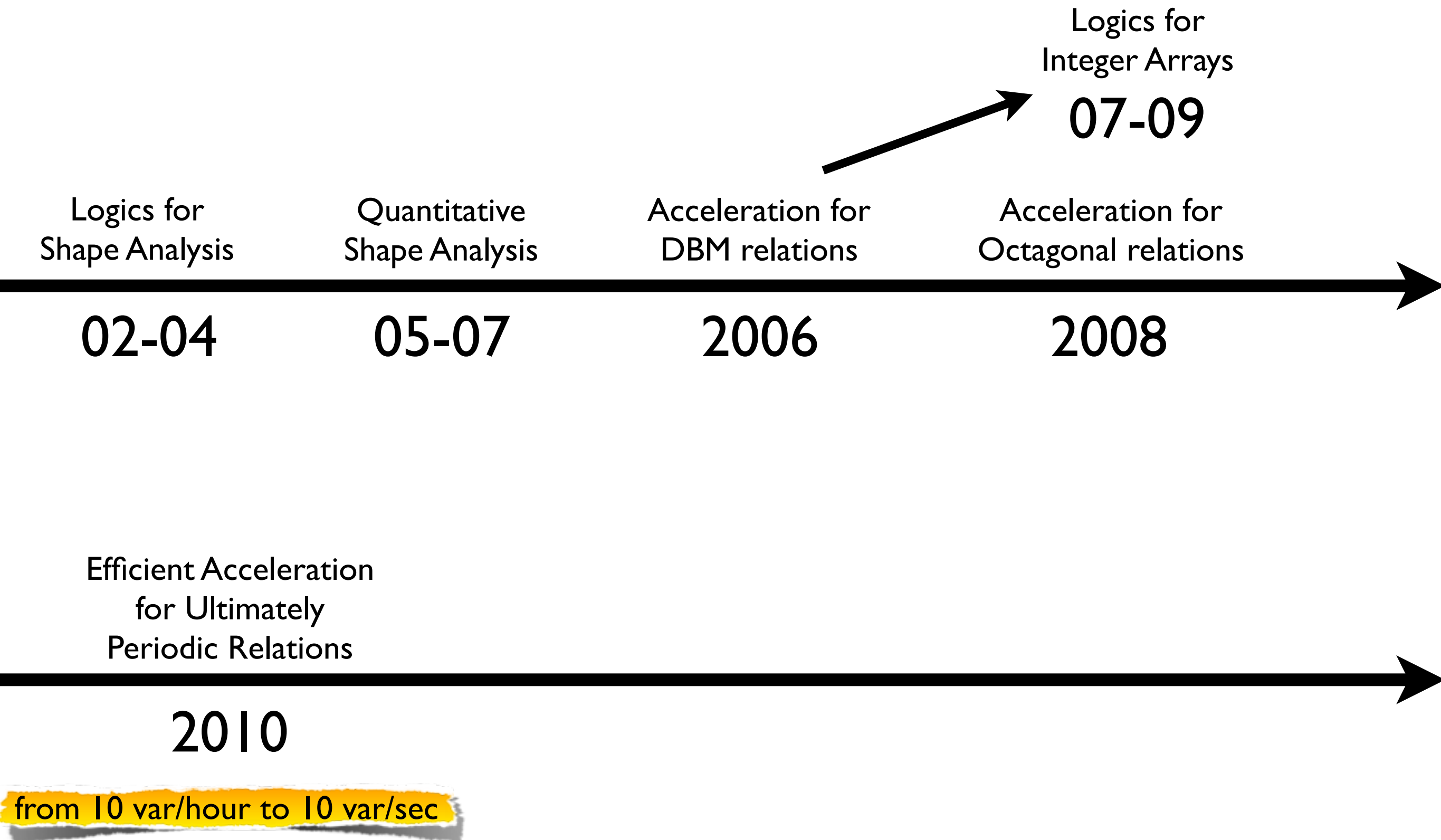
A Personal Timeline



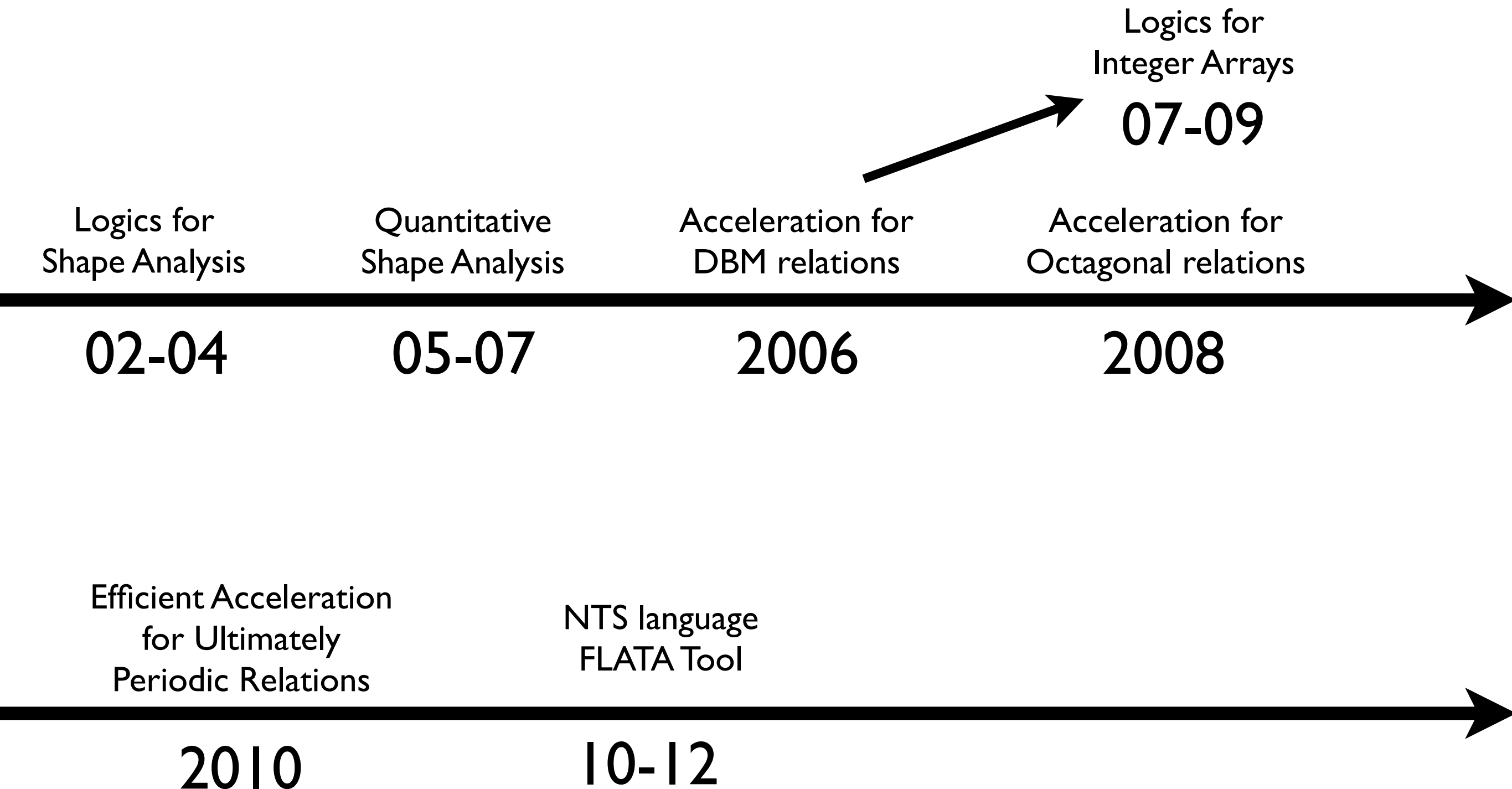
A Personal Timeline



A Personal Timeline

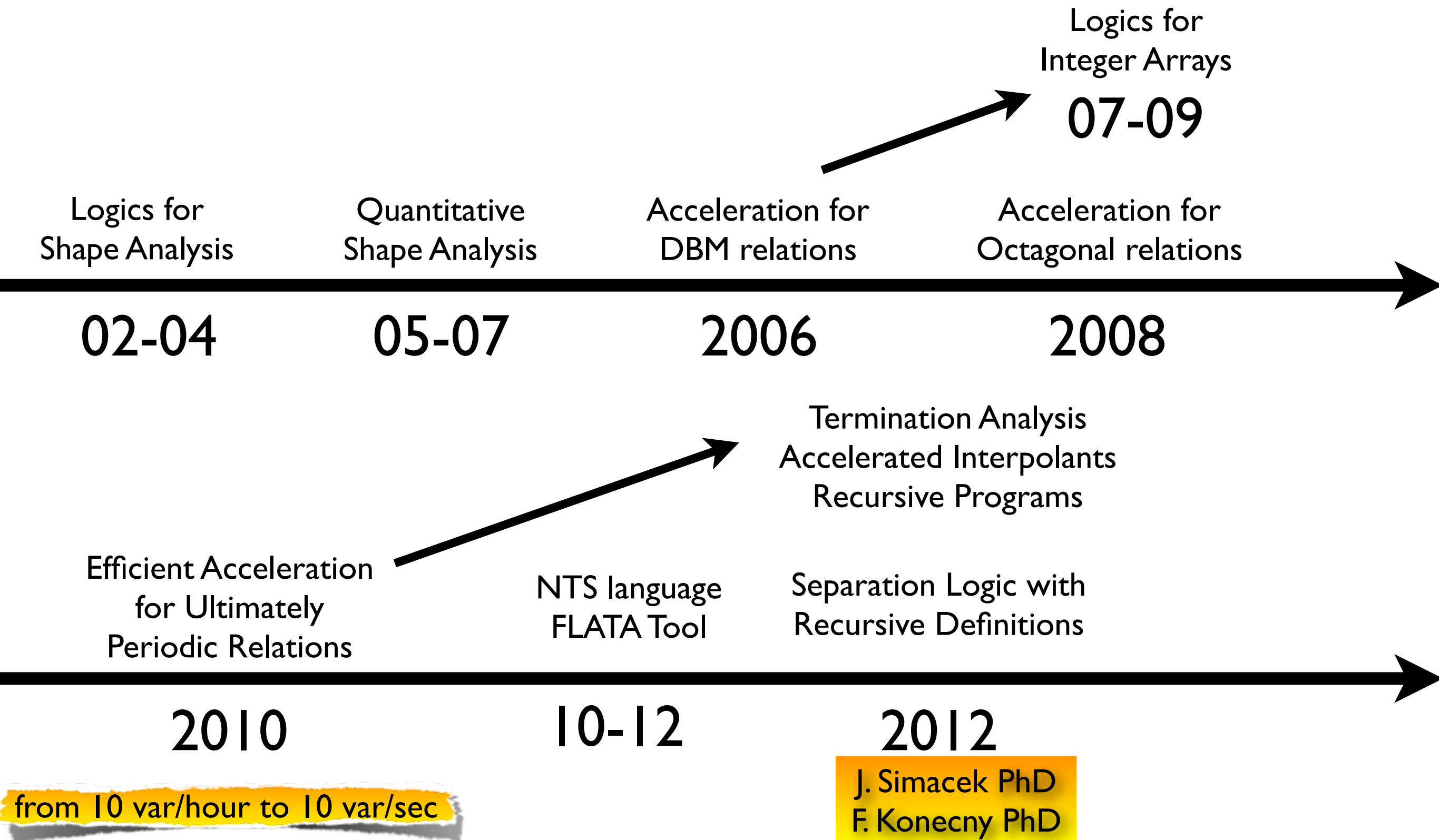


A Personal Timeline

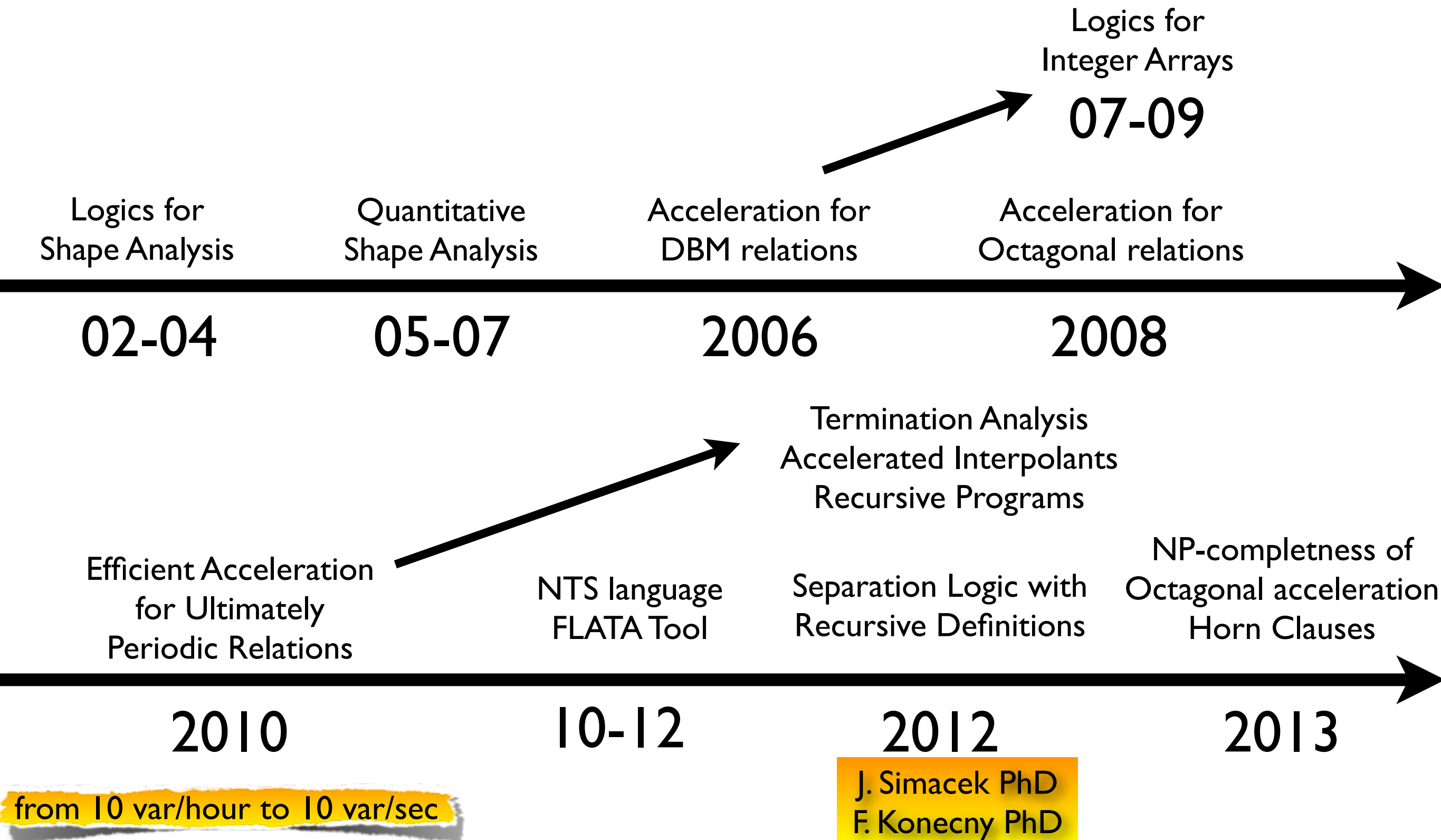


from 10 var/hour to 10 var/sec





A Personal Timeline



A Personal Timeline



Future Projects

-  Study the complexity of discrete systems from a different perspective (algorithmic entropy)
-  Computational complexity of temporal logic for discrete infinite state systems
-  Compositional shape analysis based on Separation Logic
-  Multi-level program analysis (axiomatic vs. imperative)

Projects and Collaborations

- 📌 AVERILES (RNTL 2006-2009)
- 📌 VERIDYC (ANR SEGI 2009-2013)
- 📌 ADEPT (ANR INS - decision pending)
- 📌 LIAFA Paris (Equipe Modelisation et Verification)
- 📌 Brno University of Technology (VeriFIT group)
- 📌 IMDEA Madrid (Pierre Ganty)
- 📌 EPFL Lausanne (LARA group), TUM (Rybalchenko group), MSR (Bjorner, Qadeer)